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APPLICATION FOR UNITED STATES LETTERS PATENT

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TITLE: IMAGE DISPLAY APPARATUS
FOR FIXING LUMINANCE OF
BLANK AREA AND VARYING
ONLY LUMINANCE OF IMAGE

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BACKGROUND OF THE INVENTION

The present invention relates to an image display apparatus.

Generally, image display apparatuses include a function for adjusting the black level, that is, the level at which the luminance is lowest in an image to be displayed on a monitor of these apparatuses. Conventionally, in order to realize this function, a method is used to vary a γ correction voltage in a γ correction circuit. This γ correction corrects the characteristics of gradation (degree of luminance variation) of an image to linear characteristics, and use of this correction also makes it possible to adjust the black level at which the luminance is lowest.

Meanwhile, there is a case in which a blank area is displayed on an image display apparatus such as that described above so that a blanking mark indicating a photographic range of a video camera, etc., is displayed superimposed on an image. This blank area is often displayed at the black level at which the luminance is

lowest. It is preferable that the black level of this blank area always be at a predetermined level without being influenced by the luminance of an image to be displayed.

However, if attempts to vary the black level by a method which uses the above-described γ correction circuit are made, since this γ correction circuit is provided immediately before a driver which drives a display mechanism, such as an LCD, and a combined image after the blank area and the image are combined together is corrected, there is a problem in that the luminances of both of the blank area and the image vary at the same time.

SUMMARY OF THE INVENTION

The present invention has been achieved to solve the above-described problem. An object of the present invention is to provide an image display apparatus capable of fixing the luminance of a blank area and varying only the luminance of an image.

To achieve the above-mentioned object, according to the present invention, there is provided an image display apparatus comprising an A/D converter to convert an input analog image signal into digital image data; a black level setting mechanism to set the black level of the digital image data by adjusting a lower-limit reference voltage of the A/D converter; a blank data generator to generate blank

data to display a blank area around an image display area on a screen; an image data combiner to combine blank data generated by this blank data generator and digital image data output from the A/D converter; and a display to display an output of this image data combiner on the screen.

According to the image display apparatus of the present invention, the black level of an image display area can be adjusted by a black level setting mechanism independently of the data of the blank area.

Preferably, the black level setting mechanism is a variable resistor. The black level setting mechanism preferably includes an illuminance sensor to detect the illuminance of the surroundings of a video camera, which outputs an analog image signal so that the black level is automatically set in correspondence with the illuminance of the surroundings of the camera.

The automatic setting of the black level is complete since the illuminance sensor outputs a lower-limit reference voltage corresponding to the detected illuminance .

The above and further objects, aspects and novel features of the invention will become more fully apparent from the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram of an image display apparatus according to a first embodiment of the present invention;

Fig. 2 is a diagram of circuits peripheral to an A/D converter;

Fig. 3 is a diagram showing the relationship between an image display of an LCD and a combined image signal;

Fig. 4 is a timing chart of a video signal; and

Fig. 5 is a schematic diagram of an image display apparatus according to a second embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The construction of an image display apparatus 1, which is a programmable logic device (PLD), according to a first embodiment of the present invention is described below with reference to Fig. 1. The image display apparatus 1 is provided with input terminals 1a, 1b, and 1c for inputting a video signal from the outside. Also, the image display apparatus 1 has contained therein a Y/C separation RGB decoding circuit 2, an A/D converter 3, a variable resistor 6, an image signal processing circuit 7, a gate driver 13, a source driver 14, a γ correction circuit 15, a 6-inch high-resolution TFT LCD 16 having 962×562 pixels, a backlight 17, and an inverter 18.

The input terminal 1a is connected to the input terminal of the Y/C separation RGB decoding circuit 2, and the output terminal of the Y/C separation RGB decoding circuit 2 is connected to the input terminal of the A/D converter 3. The input terminals 1b and 1c are connected directly to the input terminal of the A/D converter 3.

The variable resistor 6 has three terminals, a second terminal thereof extending from the middle of the resistor so as to allow variation of the connection point with the resistor. The first and third terminals extend from both ends of the resistor. Therefore, the resistance value between the first terminal and the second terminal, and the resistance value between the second and the third terminal are variable. The second terminal is connected to the input terminal of the A/D converter 3. The first terminal is fixed to an upper-limit reference voltage V_h , and the third terminal is connected to a ground potential.

The output terminal of the A/D converter 3 is connected to the input terminal of the image signal processing circuit 7. The output of this image signal processing circuit 7 is connected to the input terminals of the gate driver 13 and the source driver 14. The output terminal of the γ correction circuit 15 is connected to the input terminal of the source driver 14.

The output terminals of the gate driver 13 and the

Referring also to Fig. 1, the internal construction of the A/D converter 3 is described below. The A/D converter 3 has contained therein a clamping circuit 4 and an A/D conversion circuit 5. The three input terminals provided in the A/D converter 3 are connected to the input terminal of the clamping circuit 4, and the output terminal of this clamping circuit 4 is connected to the input terminal of the A/D conversion circuit 5. The output terminal of the A/D conversion circuit 5 is connected to the output terminal of the A/D converter 3. The input terminal of the A/D converter 3, which is connected to the second terminal of the variable resistor 6, is connected to the input terminal of the lower-limit reference voltage of the A/D conversion circuit 5.

Referring also to Fig. 1, the internal construction of the image signal processing circuit 7 is described below. The image signal processing circuit 7 has contained therein

an image data conversion circuit 8, a blank data generation circuit 9, a blanking marker generation circuit 10, an image data combining circuit 11, and an LCD controller 12.

The input terminal of the image signal processing circuit 7 is connected to the input terminal of the image data conversion circuit 8. The output terminals of the image data conversion circuit 8, the blank data generation circuit 9, and the blanking marker generation circuit 10 are connected to the input terminal of the image data combining circuit 11. The output terminal of the image data combining circuit 11 is connected to the input terminal of the LCD controller 12, and the output terminal of this LCD controller 12 is connected to the output terminal of the image signal processing circuit 7.

Next, referring to Fig. 2, a detailed circuit construction of the periphery of the A/D converter 3 is described. A video signal from the input terminal of the image display apparatus 1 or from the output terminal of the Y/C separation RGB decoding circuit 2 is input to a terminal Vin of the A/D converter 3 through a capacitor 19. A clock signal is input to a terminal CLK of the A/D converter 3. A clamping pulse is input to a terminal CLP of the A/D converter 3. A clamping voltage is input to a terminal Vref of the A/D converter 3.

A lower-limit reference voltage output from the second

terminal of the variable resistor 6, which is connected to a reference voltage source 20 output from the second terminal of the variable resistor 6, is input to the terminal V_l of the A/D converter 3. An upper-limit reference voltage, which is output from the reference voltage source 20 through a variable resistor 21, is input to a terminal V_h of the A/D converter 3. The output terminal on the negative side of the reference voltage source 20 is connected to a ground potential. An 8-bit digital signal is output from the output terminals D₀ to D₇ of the A/D converter 3. This digital signal takes a digital value such that the section between the lower-limit reference voltage and the upper-limit reference voltage is divided evenly by 256, that is, an 8-bit digital value.

Next, referring to Fig. 1, the operation of this embodiment is described. A video signal, which is an analog signal, is input from the input terminals 1a, 1b, or 1c provided in the image display apparatus 1. In a case where a video signal is input from the input terminal 1a, this video signal is input to the A/D converter 3 after passing through the Y/C separation RGB decoding circuit 2. In a case where a video signal is input from the input terminal 1b or 1c, the input video signal is input directly to the A/D converter 3.

The black level, that is, the level at which luminance

The digitized video signal, which is input to the image signal processing circuit 7, is converted into image data by the image data conversion circuit 8 contained in the image signal processing circuit 7, and is input to the image data combining circuit 11. Blank data output from the blank data generation circuit 9 contained also in the image signal processing circuit 7 is also input to the image data combining circuit 11. This blank data contains a signal that specifies a black level in a blank area on the screen.

Furthermore, a blanking marker signal output from the blanking marker generation circuit 10 is also input to the image data combining circuit 11. This blanking marker signal contains a signal that specifies a white level (level at which the luminance is highest) of a boundary line between the image display area of the screen and the blank area thereof. The image data combining circuit 11 combines the image data, the blank data, and the blanking marker signal, and outputs the combined image data to the LCD controller 12.

The γ correction circuit 15 sends a γ correction voltage to the source driver 14 so that γ correction of the image is performed. Also, the inverter 18 drives the backlight 17 so that this backlight 17 supplies transmission illumination light from the back of the LCD 16.

A waveform of combined image data (video signal) to display a particular line 16d in the horizontal direction on the screen 16a is shown at (a) in Fig. 3. In this

A first interval A of the line 16d is drawn by an interval A' of a video signal, an interval B is drawn by an interval B', and an interval C is drawn by an interval C'. The signal level of the interval A' and the interval C' is a black level determined in accordance with the blank data generated by the blank data generation circuit 9.

The blank areas displayed in the upper and lower portions of the screen 16a are displayed by the line at this

The black level of the blank area 16c differs from the black level of the image display area 16b, each of which is determined by a mutually different signal. That is, the black level of the blank area 16c is determined by the blank data generated by the blank data generation circuit 9, and the black level of the image display area 16b is determined by the lower-limit reference voltage input to the terminal V1 of the A/D converter 3. The variable resistor 6 adjusts the lower-limit reference voltage .

Since the blank data generated by the blank data generation circuit 9 does not pass through the A/D converter 3, even if the lower-limit reference voltage is changed, this blank data is not affected by this change. Therefore, even if the lower-limit reference voltage is adjusted by the variable resistor 6 and the black level of the image display area 16b is adjusted, the black level of the blank area 16c does not change.

Next, referring to Fig. 4, a sampling operation of a video signal is described. The black level (the level at which the luminance is lowest) of the input video signal is determined by the clamping voltage, which has been input to the terminal Vref when a clamping pulse is input to the CLP terminal of the A/D converter 3. The digital signal output

from the A/D converter 3 becomes a value determined by the relationship between the clamping voltage and the lower-limit reference voltage input to the terminal V1 of the A/D converter 3. The sampling of the video signal is performed in synchronization with the clock signal input to the terminal CLK of the A/D converter 3.

Next, referring to Fig. 5, a second embodiment of the present invention is described. The same components in Fig. 5 as those of the first embodiment are given the same reference numerals, and accordingly, descriptions thereof are omitted. In the second embodiment, instead of the variable resistor 6 in the first embodiment, an illuminance sensor 23 and a lower-limit reference voltage generation circuit 22 are provided. The illuminance sensor 23 is disposed, for example, near a video camera or the like which outputs a video signal to be input to the image display apparatus 1, and measures the illuminance near this video camera or the like. The output of the illuminance sensor 23 is input to the lower-limit reference voltage generation circuit 22, whereby a lower-limit reference voltage corresponding to this input is output from the lower-limit reference voltage generation circuit 22, and this output is input to the A/D conversion circuit 5 inside the A/D converter 3.

With such a construction, the lower-limit reference

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